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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,670	03/06/2002	Donald C. Soltis JR.	10016628-1	3827

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,670	SOLTIS ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed urgency indicator being based upon expected progress of a thread within the pipeline execution units and the claimed urgency indicator being based upon expected progress of a thread within the pipeline execution units must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

2. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Keckler, Stephen W., et al., Concurrent Event Handling through Multithreading, 1999, IEEE Transactions on Computers, volume 48, NO. 9, pages 903-916 (hereinafter "Keckler et al.").

5. Referring to claim 1, Keckler et al. have taught a method for determining thread switch points within pipeline execution units of a processor, comprising the steps of:

a. monitoring instruction processing of a first thread within the pipeline execution units (page 908, left hand column, Monitors availability of instruction register operands.);

b. in the event of a possible switch point within the pipeline execution units, deactivating the first thread, or not, based upon a first urgency indicator for the first thread (page 908, left hand column, Each cycle the synchronization stage determines which instructions from each thread to activate and execute based on arrived data and associated instruction priorities.), the first urgency indicator being based upon progress of the first thread within the pipeline execution units (page 908, left hand column, The first urgency indicator, or the indicator that indicates whether all of the data for the instruction has arrived, is based upon the progress of the thread within the pipeline execution units. When all of the data for an instruction is not available, the thread is not able to progress past the synchronization stage in the pipeline.).

6. Referring to claim 2, Keckler et al. have taught a method of claim 1, as described above, and further comprising deactivating the first thread and activating a second thread based upon a second urgency indicator for the second thread (page 908, left hand column, An important higher priority thread is now ready to execute and monopolizes the system.), the second urgency indicator being based upon expected progress of the second thread with the pipeline execution units (page 908, left hand column, A high priority thread is expected to progress through the pipeline execution units quicker than lower priority threads.).

7. Referring to claim 3, Keckler et al. have taught a method of claim 2, as described above, and further comprising deactivating the second thread, or not, based upon the second urgency indicator for the second thread and in the event of a possible switch point event of the second thread (page 908, left hand column, Each cycle instructions are scheduled for each thread depending on the respective priorities.).

8. Referring to claim 4, Keckler et al. have taught a method of claim 3, as described above, and further comprising activating another thread within the pipeline if the second thread is switched out (page 908, left hand column, If the input data for a high priority instruction is not available, another ready instruction from a different thread is activated and executed.).

9. Referring to claim 5, Keckler et al. have taught a method of claim 1, as described above, and the step of deactivating the first thread comprising deactivating the first thread, or not, based upon the first urgency indicator and upon a second urgency indicator of a second thread (page 908, left hand column, An important higher priority thread that is now ready to execute monopolizes the system.), the second urgency indicator being based upon expected progress of the second thread within the pipeline execution units (page 908, left hand column, A high

priority thread is expected to progress through the pipeline execution units quicker than lower priority threads.).

10. Referring to claim 6, Keckler et al. have taught a method of claim 1, as described above, and the step of monitoring comprising utilizing a thread controller coupled with the execution units (page 908, left hand column, Synchronization stage).

11. Referring to claim 7, Keckler et al. have taught a method of claim 1, as described above, and further comprising modifying the first urgency indicator to increase or alternatively decrease urgency of the first thread based upon characteristics associated with the switch event (page 908, left hand column, An instruction can only stall for a maximum of 255 cycles and then is given a higher priority and is allowed to execute.).

12. Referring to claim 8, Keckler et al. have taught a method of claim 7, as described above, and further comprising determining whether a time slice expiration occurred (page 908, left hand column, The time slice is 255 cycles.).

13. Referring to claim 9, Keckler et al. have taught a method of claim 8, as described above, and further comprising utilizing a time slice expiration unit (page 908, left hand column, See preempt state, idle cycle counters, and limit registers.).

14. Referring to claim 10, Keckler et al. have taught a method of claim 7, as described above, and further comprising determining whether a cache miss occurred (Page 909, right hand column).

15. Referring to claim 11, Keckler et al. have taught a method of claim 7, as described above, and further comprising inserting an instruction to the pipeline to change urgency of the thread (page 908, Changing the urgency of the thread is inherently performed by an instruction.).

16. Referring to claim 12, Keckler et al. have taught a method of claim 1, as described above, and further comprising the steps of deactivating the first thread and activating a second thread, and modifying urgency of the second thread (page 908, left hand column, As soon as a high priority thread is ready to execute, the high priority instruction increases the urgency of the thread and monopolizes the system.).

17. Referring to claim 13, Keckler et al. have taught a method of claim 1, as described above, and further comprising the steps of monitoring possible switch points of an inactive thread having a second urgency indicator that is based upon expected progress of the inactive thread within the pipeline execution units (page 908, left hand column, A second urgency indicator is the instruction thread priority indication of Keckler. A high priority thread is expected to progress through the pipeline execution units quicker than lower priority threads.), and deactivating the first thread, or not, based upon a first and second urgency indicator (page 908, left hand column, The time slice is 255 cycles, This is performed on a cycle-by-cycle basis.).

18. Referring to claim 14, Keckler et al. have taught a processor for processing multi-threaded program instructions, comprising:

a. an array of pipeline execution units and associated heuristics affecting how the instructions are processed within the units (page 904, left hand column, page 908); and

b. a thread controller for monitoring processing of the instructions within the units and for switching between multiple program threads based upon (a) the heuristics and (b) urgencies of the program threads (page 908, left hand column, Switch between multiple program threads based on (a) the time slice duration of 255 cycles, or the heuristics, and (b) the thread priorities, or the urgencies of the program threads.),

wherein the urgencies are based upon one or both of (a) progress of the threads through the pipeline execution units (page 908, left hand column, The first urgency indicator, or the indicator that indicates whether all of the data for the instruction has arrived, is based upon the progress of the thread within the pipeline execution units. When all of the data for an instruction is not available, the thread is not able to progress past the synchronization stage in the pipeline.) and (b) expected progress of the program threads through the pipeline execution units (page 908, left hand column, A high priority thread is expected to progress through the pipeline execution units quicker than lower priority threads.).

19. Referring to claim 15, Keckler et al. have taught a processor of claim 14, as described above, and the heuristics comprising one or more of time slice expiration heuristics, cache miss heuristics and processor interrupt heuristics (page 908, left hand column, The time slice is 255 cycles.).

20. Referring to claim 16, Keckler et al. have taught a processor of claim 14, as described above, and the program threads comprising one or more instructions, one of the instructions changing urgency for at least one thread of the processor (page 908, left hand column, A higher priority instruction becomes ready to execute and the urgency of the instruction increases, thereby effectively decreasing urgency of the other threads.).

21. Referring to claim 17, Keckler et al. have taught a processor of claim 14, as described above, and the controller modifying an urgency of any of the threads to modify future treatment of the threads in switch out events (page 908, left hand column, When a thread has been idle for 255 cycles, the urgency of the instruction is modified in order to allow the thread to execute.).

22. Referring to claim 18, Keckler et al. have taught a processor of claim 17, as described above, and the controller either decreasing or increasing urgency for the program threads by injecting an instruction to the pipeline execution units (page 908, Changing the urgency of the thread is inherently performed by an instruction.).

23. Referring to claim 19, Keckler et al. have taught a processor of claim 12, as described above, and further comprising a time slice expiration unit for monitoring expiration of threads within the processor (page 908, left hand column, The time slice is 255 cycles. See preempt state, idle cycle counters, and limit registers.).

Response to Arguments

24. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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